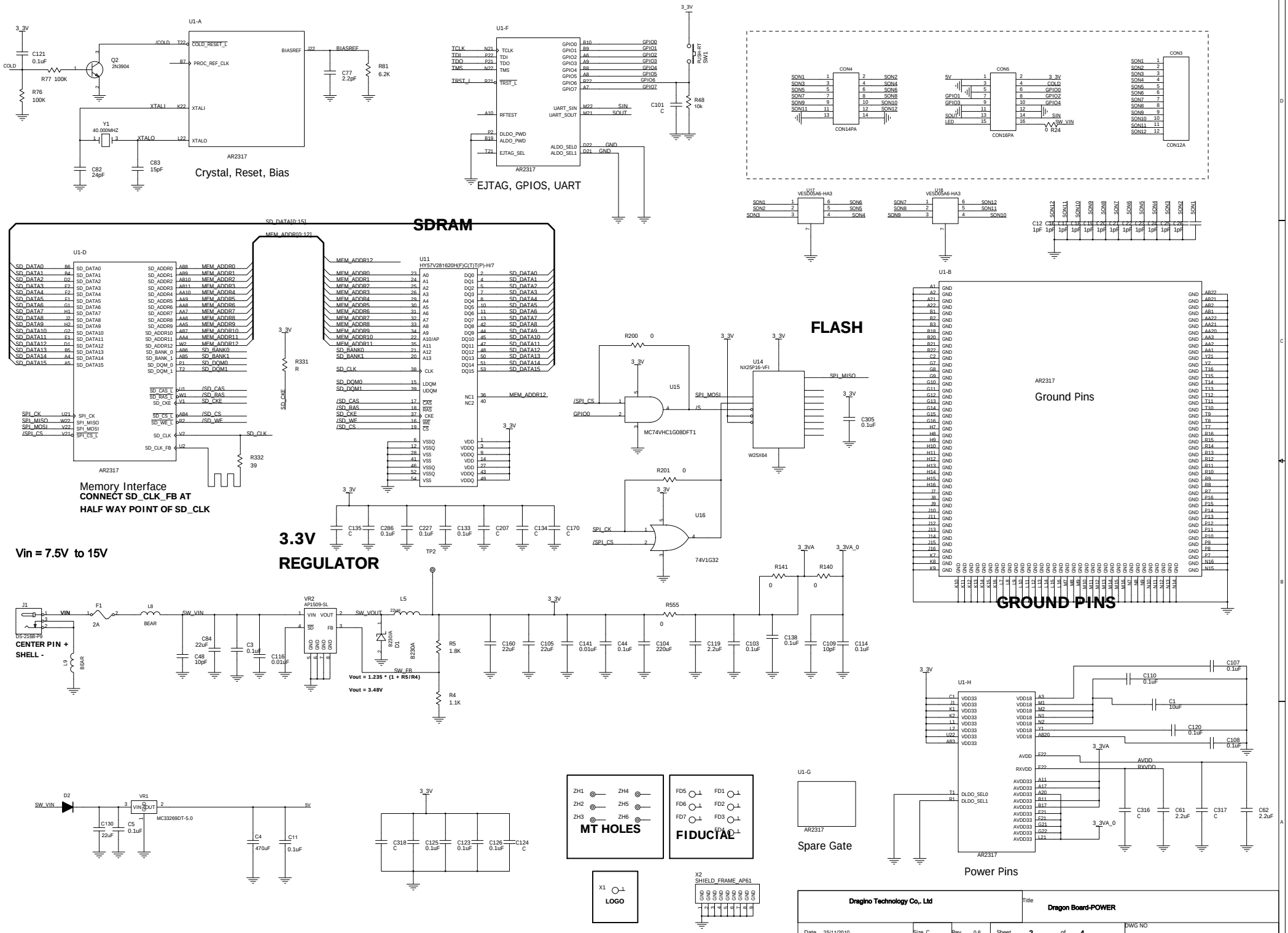
DATE	REVISION NUMBER	INITIALS	DESCRIPTION
24/05/10	**Ver 0.1**		change SDRAM and RAM change xz1401 to AP1509 change ethernet to rtl8201c add 12-position screw terminal add ESD protection (e.g. 2xMAX3206E) del LAN add SIN and SOUT to CON5 change LED1 and LED2 to CON5 change 5V instead 3.3V for MAX3206E change vin to 7.5v ~15V add Vin to CON5 change GPIO6 connect to reset buttom add LED 5pcs
28/05/10	Ver 0.2		change vesd05a6-ha3 for ESD add R41 from GPIO4 to 3.3v
28/05/10	Ver 0.3		Del R41
25/06/10	Ver 0.4		Del LED1
2/07/10	Ver 0.5		change Vin to SW_Vin change CON4 CON5
25/11/10	Ver 0.6		change VR1 to mc33269dt-5.0 change RJ45 to RJ111BE provide pads on SON1-SON12 to load a small cap in parallel to GND
	Ver 0.6		Rename LED2 to LED Add 0 ohm resistor in series between the SW_VIN line and pin 16 on CON5 add a Schottky between SW_VIN and the LDO input Add L8 and L9 for EMI Del U15 and U16 add R26 R27 R28 R29

Dragino Ver 0.6

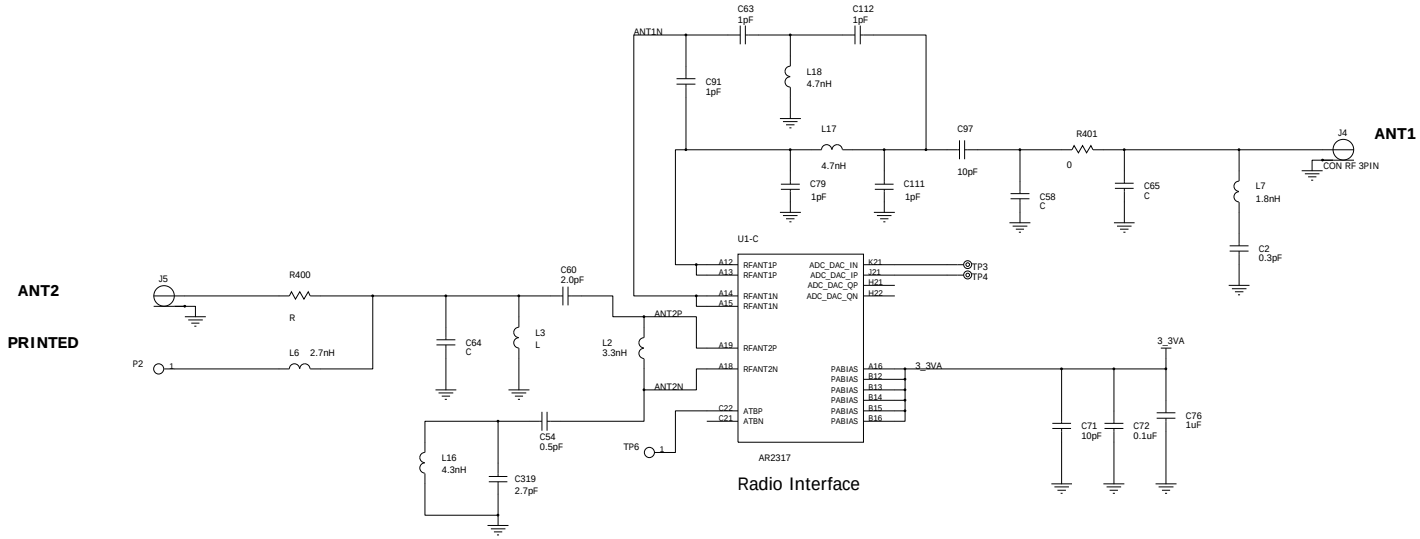
PRELIMINARY

Dragino design by:
Dragino R&D team [dragino.com]
Bart Van Der Meerssche [flukso.net]
David Rowe [rowetel.com]

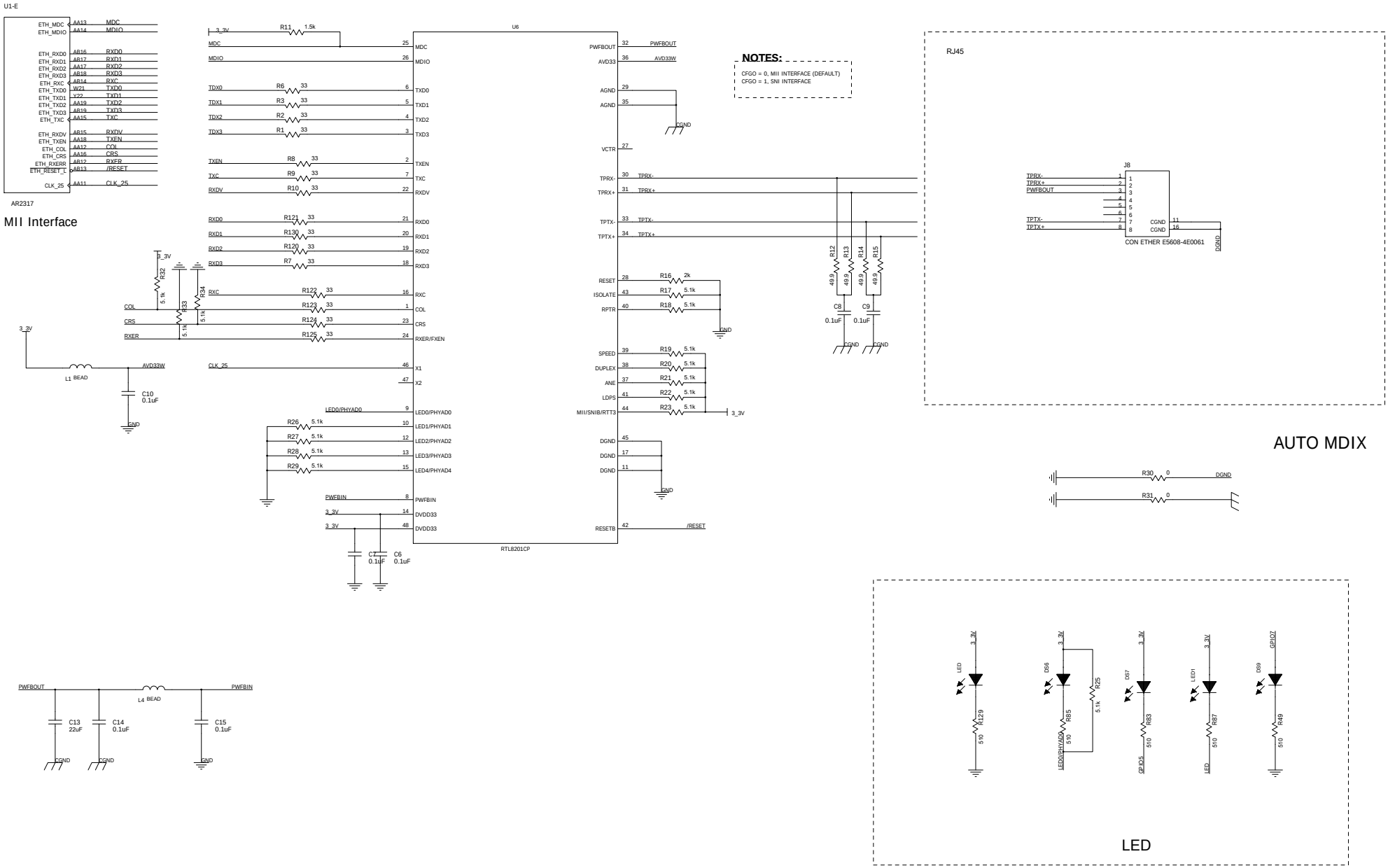
Dragino Technology Co,. Ltd					Title: Dragon Board	
Date: 25/11/2010	Size: C	Rev: 0.6	Sheet: 1 of 4			DWG NO


Crystal, Reset, Bias
EJTAG, GPIOS, UART
SDRAM
Memory Interface
CONNECT SD_CLK_FB AT
HALF WAY POINT OF SD_CLK
FLASH
Ground Pins
3.3V
REGULATOR
Vin = 7.5V to 15V
GROUND PINS
CENTER PIN +
SHELL -
Vout = 1.235 * (1 + R5/R4)
Vout = 3.48V
MT HOLES
FIDUCIAL
Spare Gate
Power Pins
LOGO
Dragino Technology Co,. Ltd
Dragon Board-POWER
Date 25/11/2010
Size C
Rev 0.6
Sheet 2 of 4

Note : Add 1 uF Cap



Dragino Technology Co,. Ltd				Title: Dragon Board - RF	
Date 25/11/2010	Size C	Rev 0.6	Sheet 3 of 4		DWG NO



Dragino Technology Co,. Ltd			Title: Dragon Board- ETHERNET SWITCH
Date: 25/11/2010	Size: C	Rev: 0.6	Sheet: 4 of 4
			DWG NO