EC25 Reference Design

LTE Module Series

Rev. EC25_Reference_Design_Rev.E

Date: 2017-04-06

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About the Document

History

Revision	Date	Author	Description
A	2016-04-01	Winter CHEN	Initial
B	2016-08-22	Yeoman CHEN	1. Added ADC interface design in Sheet 1 2. Added power supply for codec in Sheet 3 3. Added note for UART Translator (Transistor Solution) in Sheet 4 4. Changed some DGND to AGND in audio design in Sheet 5
C	2016-10-14	Eden LIU	Added the reference design of SGMII and FC20 module
D	2016-11-11	Power JIN	1. Modified the connection of network name PCM_IN_BT and PCM_OUT_BT in Sheet 1 2. Added note 7 in Sheet 7 3. Added note 6 in Sheet 9
E	2017-04-06	Eden LIU	1. Newly opened pins 37~40 for BT UART, and removed the multiplexing between Main UART and BT UART in Sheet 1 2. Newly opened the SD card interface 3. Added the power supply control pin of SD card interface in Sheet 2 4. Modified network name TXD_MCU as RXD, RXD_MCU as TXD, CTS_MCU as CTS, RTS_MCU as RTS, RI_MCU as RI, DCD_MCU as DCD, DTR_MCU as DTR in Sheet 2 and Sheet 4 5. Modified the power supply circuit for PCM Codec in Sheet 3 6. R0904 is not mounted because SDIO_CLK in FC20 is pulled up internally

	7. Modified network name PCM_IN_BT as PCM_OUT_BT, PCM_OUT_BT as PCM_IN_BT in Sheet 1 and Sheet 9 8. Modified the unidirectional off-page connectors of SDIO_CMD, SDIO_D0, SDIO_D1, SDIO_D2 and SDIO_D3 to bidirectional ones in Sheet 1 and Sheet 9 9. Removed resistors R912, R913 and added resistor R0920 in Sheet 9 10. Added the reference design for SD card interface in Sheet 10 11. Modified the drive circuit of indicator STATUS in Sheet 11

Contents

1 Reference Design

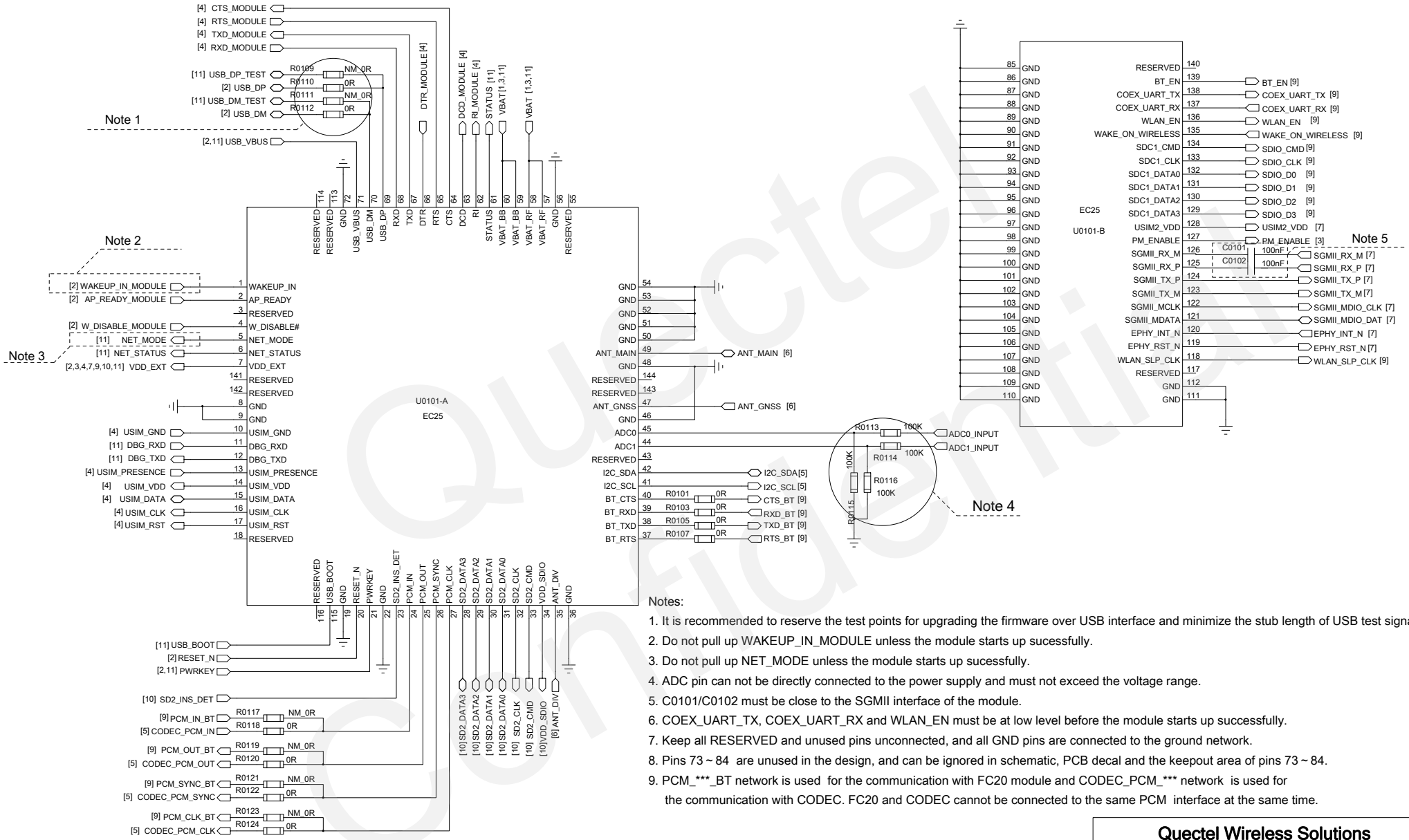
1.1. Introduction

This document provides the reference design for Quectel EC25 module.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Module Interface



Notes:

1. It is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the stub length of USB test signals.
2. Do not pull up WAKEUP_IN_MODULE unless the module starts up sucessfully.
3. Do not pull up NET_MODE unless the module starts up sucessfully.
4. ADC pin can not be directly connected to the power supply and must not exceed the voltage range.
5. C0101/C0102 must be close to the SGMII interface of the module.
6. COEX_UART_TX, COEX_UART_RX and WLAN_EN must be at low level before the module starts up successfully.
7. Keep all RESERVED and unused pins unconnected, and all GND pins are connected to the ground network.
8. Pins 73 ~ 84 are unused in the design, and can be ignored in schematic, PCB decal and the keepout area of pins 73 ~ 84.
9. PCM_***_BT network is used for the communication with FC20 module and CODEC_PCM_*** network is used for the communication with CODEC. FC20 and CODEC cannot be connected to the same PCM interface at the same time.

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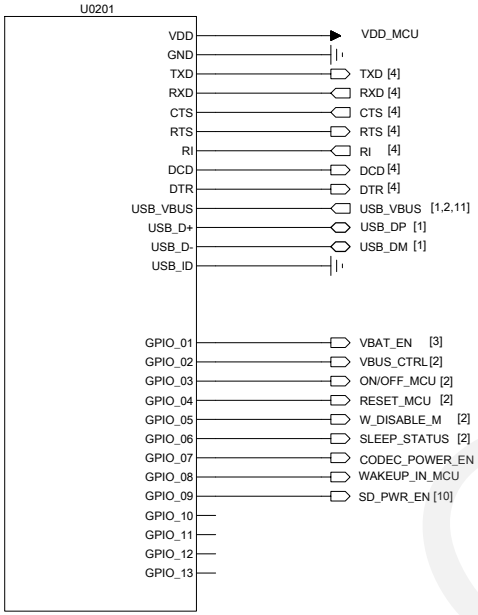
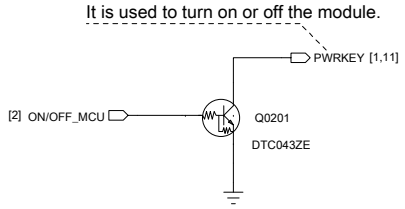
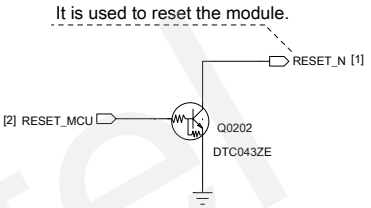
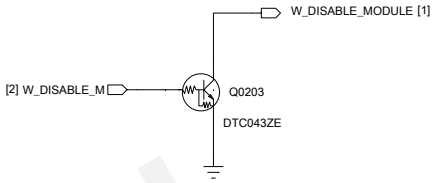
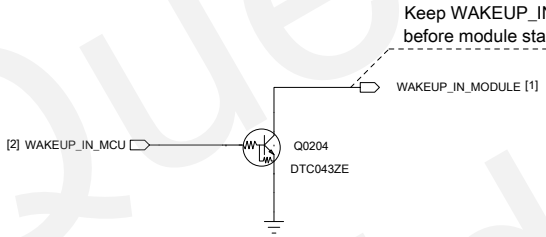
MCU Interface

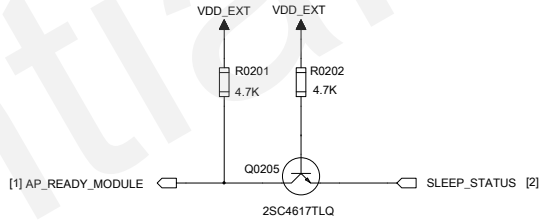




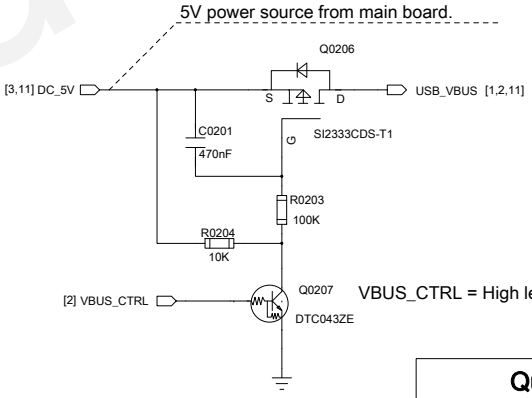








AP_READY_MODULE low level detection.



VBUS_CTRL = High level, USB_VBUS is powered on.

Notes:

1. U0201 represents customer's MCU.
2. EC25 can only work as a USB device and supports Full Speed and High Speed modes. To communicate with USB interface, MCU needs to support USB host or OTG function. The VBUS pins of MCU and EC25 should be powered by a 5V power system for USB detection, and VBUS-CTRL is used to turn on/off VBUS power supply. When VBUS_CTRL is at high level, USB_VBUS will be powered on.
3. AP_READY can be configured to high level detection and low level detection. For more details about AP_READY, please refer to *Quectel_EC25_Hardware_Design* and *Quectel_EC25&EC21_AT_Commands_Manual*.
4. Transistor circuits (Q0201~Q0205) are used for level translation.

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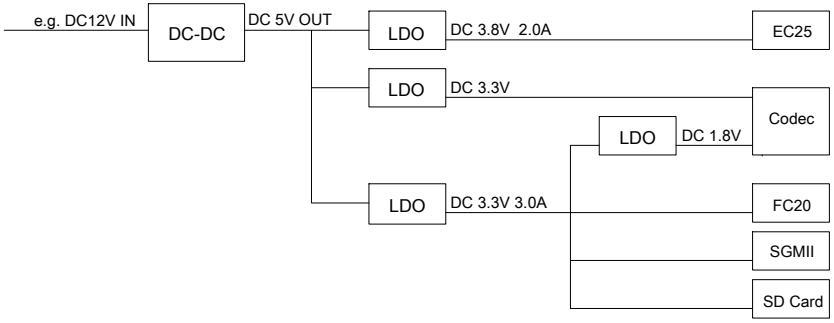
Power Supply Design

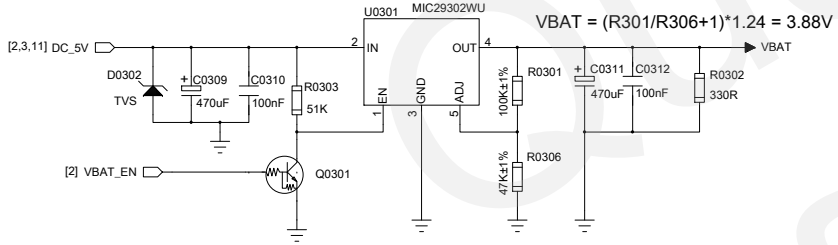
DC-DC Application

It is used when the input voltage is above 7V. Use a DC-DC converter to convert a high input voltage into 5V output, and then the LDOs will generate 3.8V, 3.3V and 1.8V typical voltages.



LDO Application

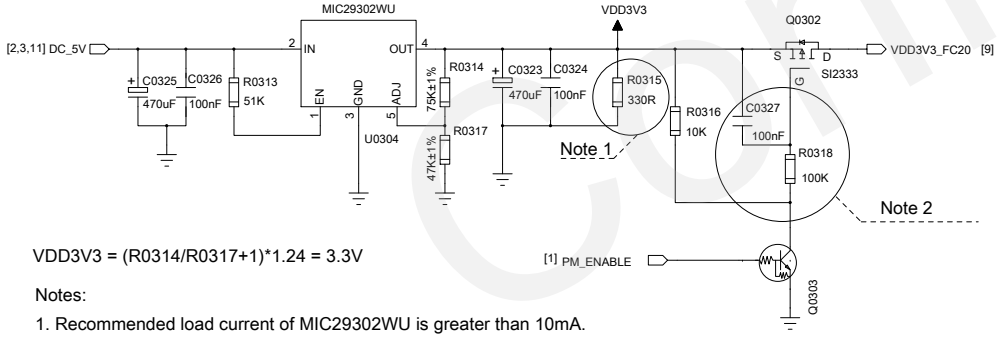
It is used when the input voltage is below 7V.



Note:

Recommended load current is greater than 10mA.

Power Supply for FC20, SGMII and SD Card

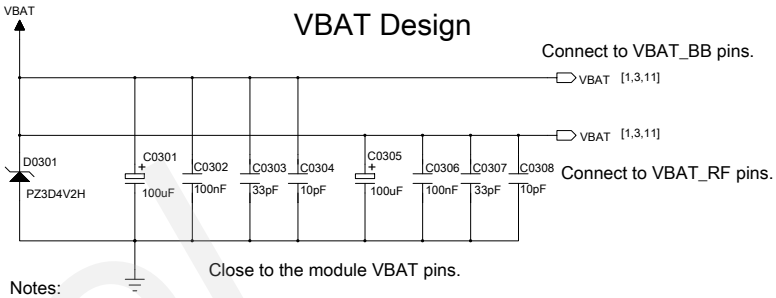


VDD3V3 = (R0314/R0317+1)*1.24 = 3.3V

Notes:

1. Recommended load current of MIC29302WU is greater than 10mA.
2. RC circuit, which is assembled with R0318 and C0327, is used to delay the start-up of MOSFET switch circuit.

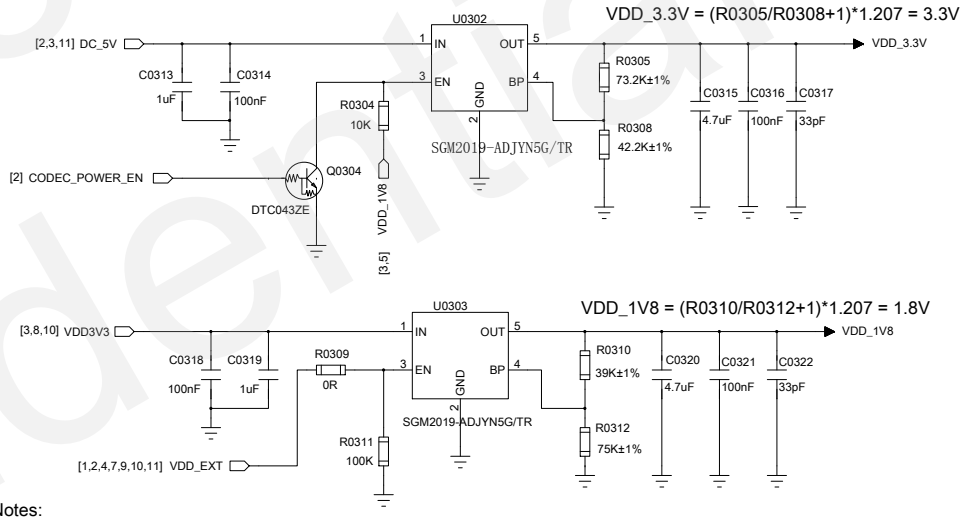
VBAT Design



Notes:

1. The power supply must be able to provide sufficient current up to 2A or more.
2. VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3V~4.3V.

Power Supply for PCM Codec



Notes:

1. CODEC_POWER_EN must be at low level in order to ensure the normal output voltage of VDD_3.3V.
   If VDD_3.3V power supply needs to be switched off, please keep CODEC_POWER_EN at high level.
2. To ensure that ALC5616 works normally, please follow the power ON and OFF sequences of its power supply.
   Power ON Sequence: power on VDD_1V8 first, then VDD_3V3.
   Power OFF Sequence: power off VDD_3V3 first, then VDD_1V8.

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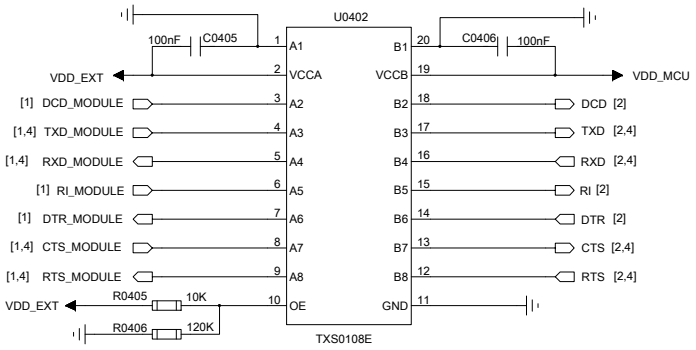
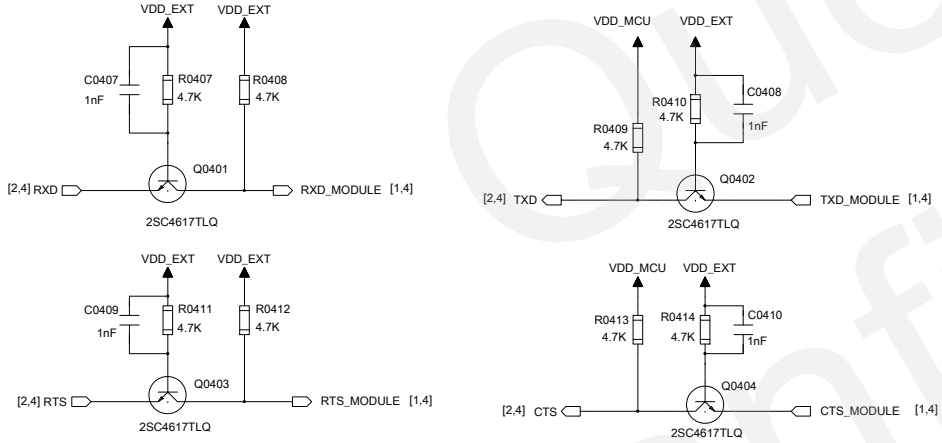
(U)SIM and UART Designs

UART Translation - IC Solution (Recommended)



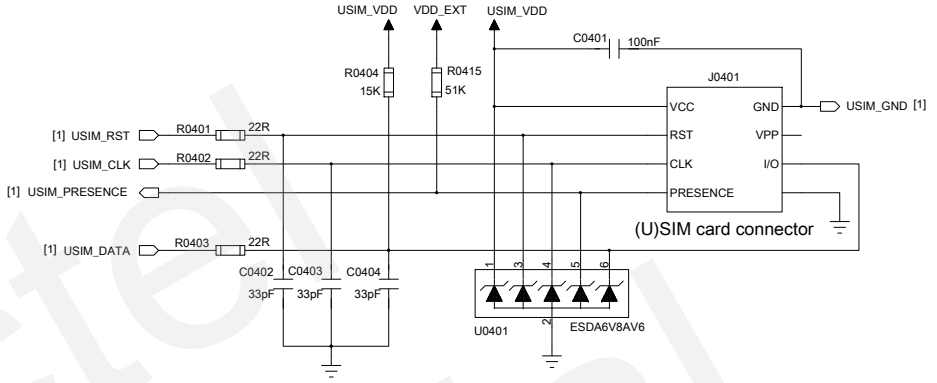
UART Translation - Transistor Solution



Notes:

1. It is recommended to use an IC conversion chip for UART translation.
   The transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.
2. The supply voltage range of VCCA should not exceed the one of VCCB.
   For more information about TXS0108E, please refer to its datasheet from TI.
3. If high baud rate needs to be enabled, it is highly recommended to install four 1nF capacitors (C0407/C0408/C0409/C0410) on transistor circuit.
4. The DTR transistor circuit is similar to the one of RTS interface.
   The RI and DCD transistor circuits are similar to the ones of CTS interface.

(U)SIM Card Interface



Notes:

1. The decouple capacitor of USIM_VDD should be less than 1uF and must be near to (U)SIM card connector.
2. EC25 module provides an input pin (USIM_PRESENCE) to detect whether the (U)SIM card exists or not.
   It supports both low level and high level detections. For more details, please refer to *Quectel_EC25_Hardware_Design*.
3. R0401~R0403 are applied to suppress the EMI spurious transmission and enhance the ESD protection.
4. It is recommended to take electrostatic discharge (ESD) protection measures near the (U)SIM card connector.
   The TVS diode with junction capacitance less than 50 pF must be placed as close as possible to the (U)SIM card connector.
5. R0404 can improve anti-jamming capability of the (U)SIM circuit and it should be placed close to the (U)SIM card connector.

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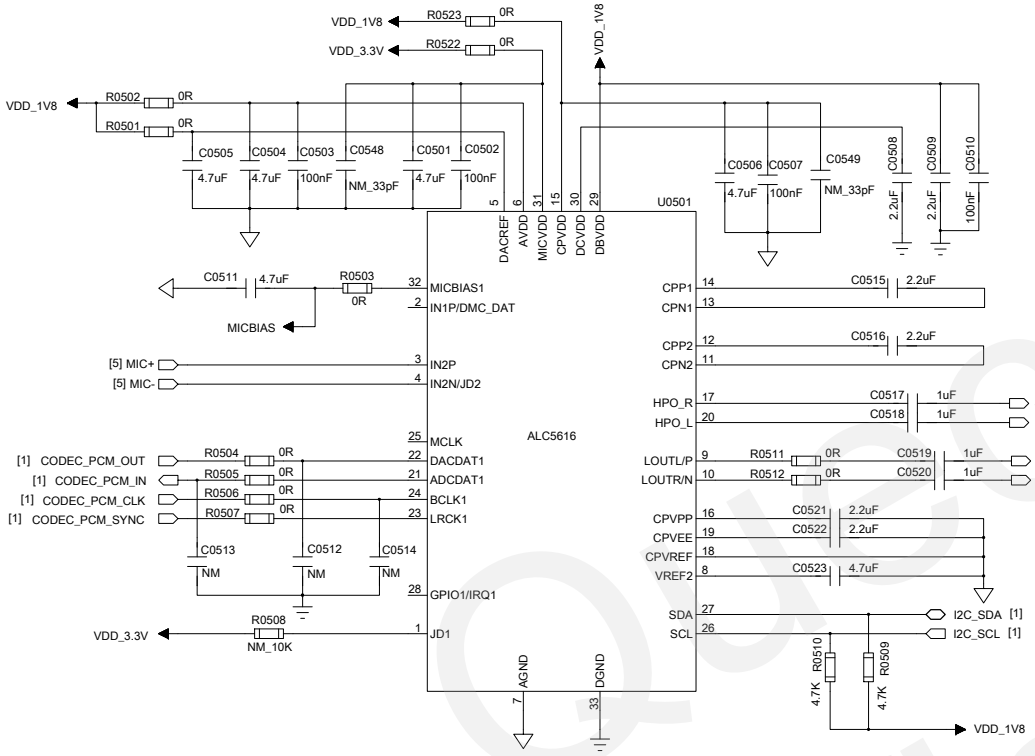
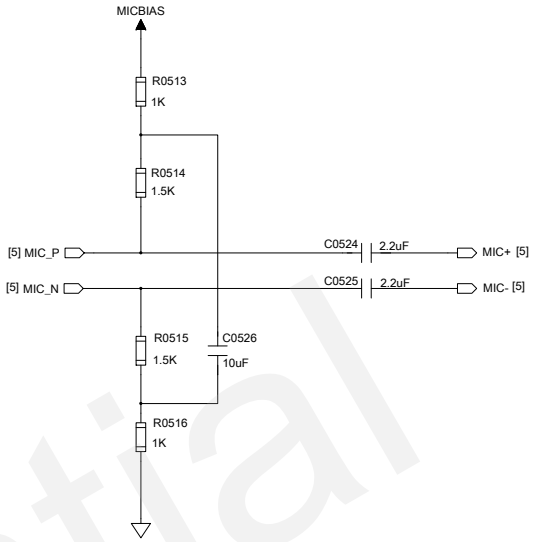
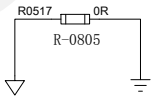
Audio Design







Note:

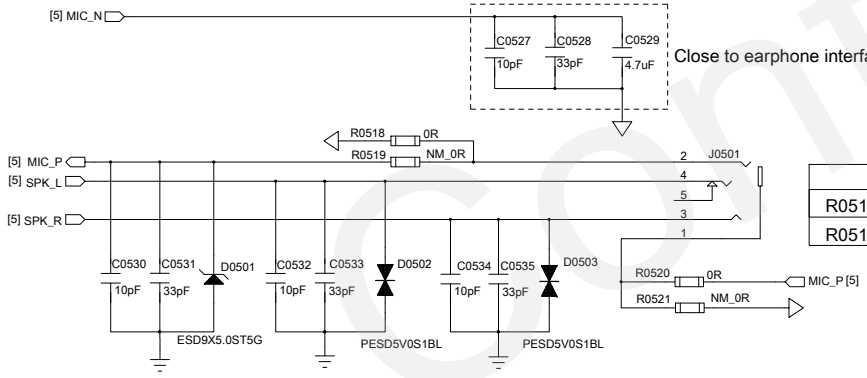
To ensure that ALC5616 works normally, please follow the power ON and OFF sequences of its power supply.

Power ON Sequence: power on DBVDD/AVDD/DACREF/CPVDD first, then MICVDD.

Power OFF Sequence: power off MICVDD first, then DBVDD/AVDD/DACREF/CPVDD.

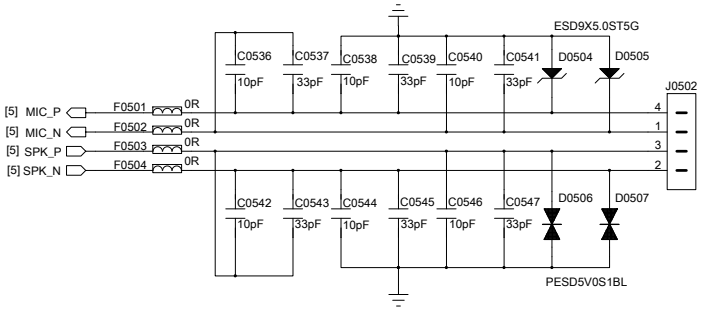
For more details, please refer to ALC5616 datasheet.

Audio - Earphone Application



	CTIA	OMTP
R0519/R0521	NM	M
R0518/R0520	M	NM

Audio - Handset Application



Notes:

1. The analog output only drives earphone and headset. For larger power loads such as speakers, the design needs to incease the audio power amplifier.
2. The maximum capacitive loading for SPK is 330 pF and the maximum capacitive loading for MIC is 250 pF.

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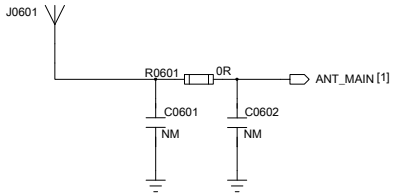
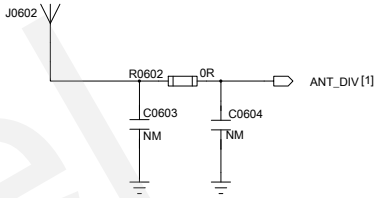
RF and GNSS Design

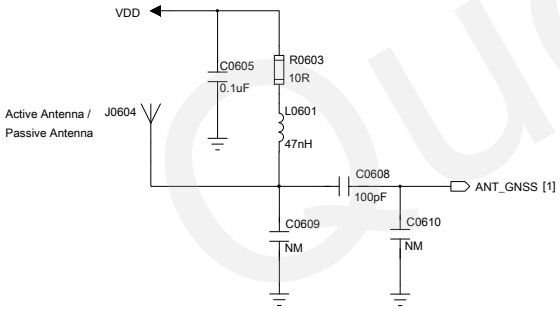
Main Antenna Interface



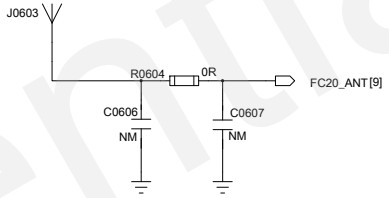
Diversity Antenna Interface



GNSS Antenna Circuit



FC20 Antenna Circuit



Notes:

1. The main antenna circuit, diversity receiving antenna circuit and FC20 antenna circuit are recommended to use PI type circuit, which is convenient for subsequent debugging.
2. The diversity reception function is ON by default. If diversity antenna is not used, there is a need to use AT command to turn off diversity reception.
3. An external LDO can be used to supply power for active antenna.
4. If antenna circuit is designed with passive antenna, R0603 and L0601 are not needed.
5. ESD protection devices should be added to the GNSS antenna interface, and the parasitic capacitance should be less than 0.05pF.
6. The impedance of the RF signal line must be controlled as 50Ω when routing.

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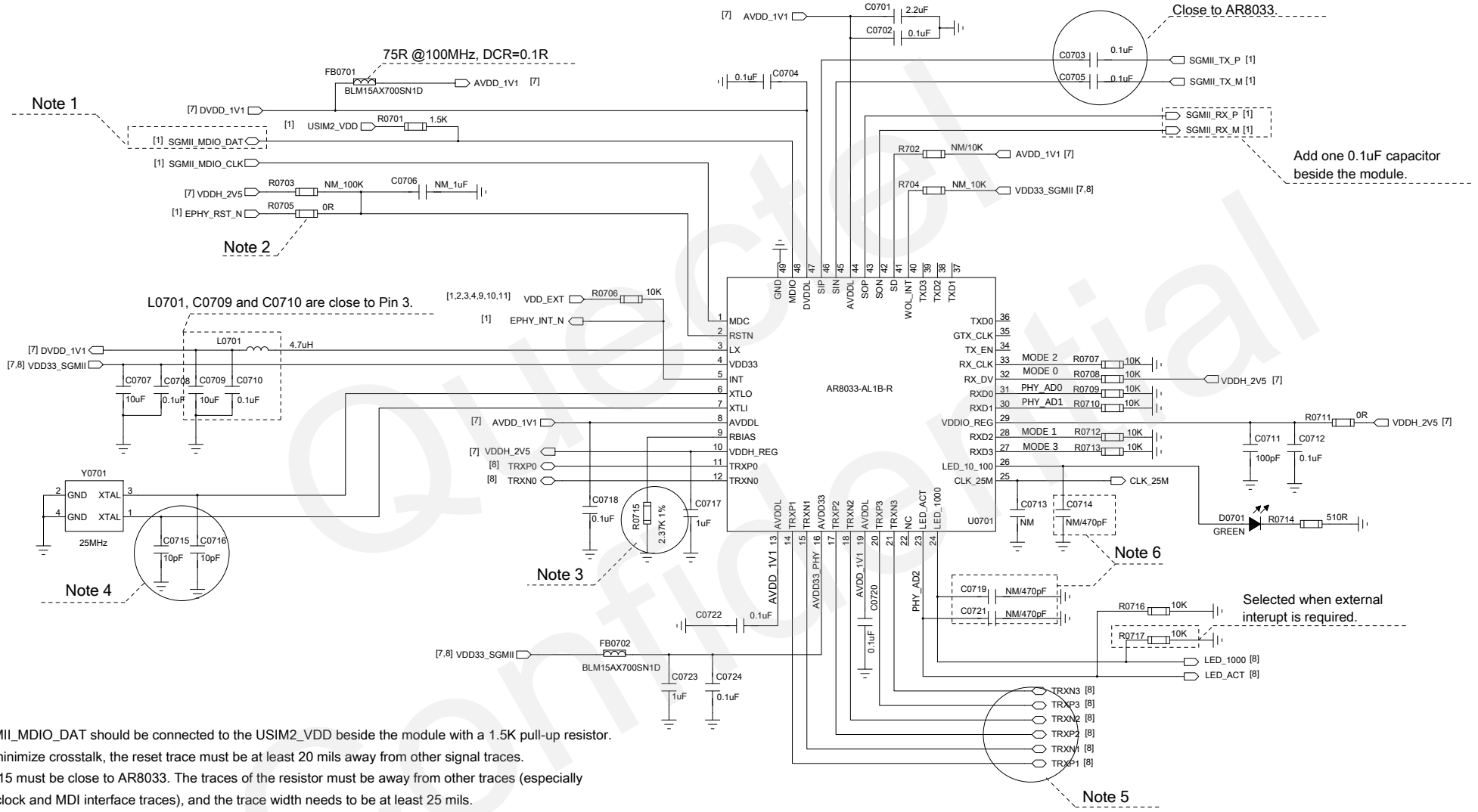
SGMII Design (Part 1)



Notes:

1. SGMII_MDIO_DAT should be connected to the USIM2_VDD beside the module with a 1.5K pull-up resistor.
2. To minimize crosstalk, the reset trace must be at least 20 mils away from other signal traces.
3. R0715 must be close to AR8033. The traces of the resistor must be away from other traces (especially the clock and MDI interface traces), and the trace width needs to be at least 25 mils.
4. The two capacitors should be selected according to the actual load capacitance of crystal and the board-level test results, at full load application temperature and voltage range.
5. The differential trace impedance of SGMII must be limited to 100Ω.
6. EMI filter is reserved. If LED pins are not used, keep C0714, C0719, C0721=470pF.
7. The space between SGMII differential pair (RX and TX traces) should be 3 times of the trace width at least. Also, SGMII should keep a distance of 3 times of its trace width from other signal lines.

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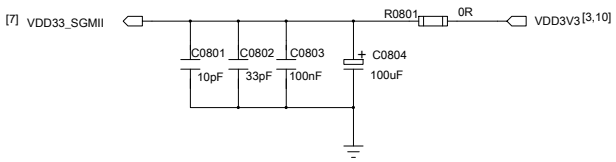
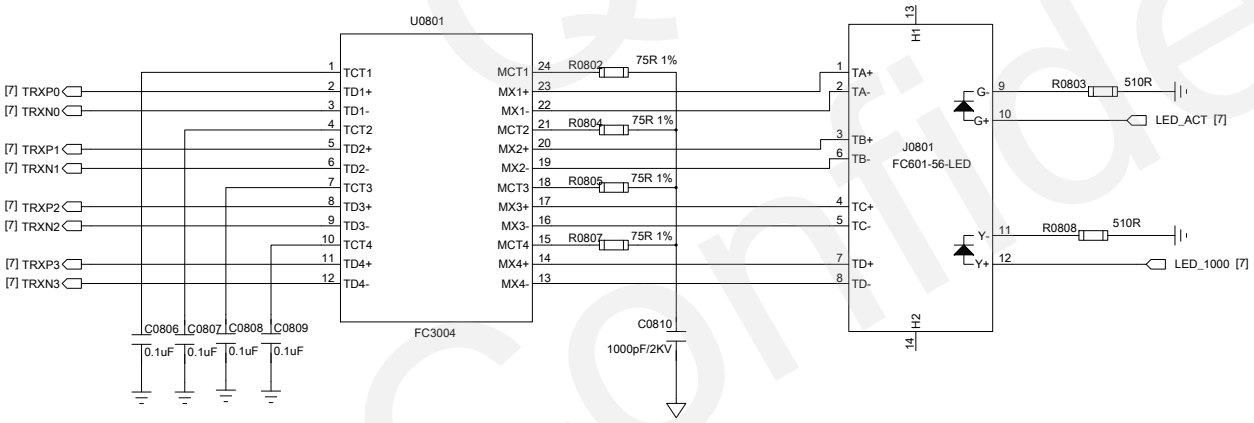
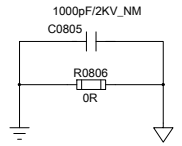
SGMII Design (Part 2)



PHY core configuration signal	Description	Default internal weak pull-up/down	Application external weak pull-up/down
PHY_AD2	PHY_AD[2:0] set the lower three bits of the physical address. The upper two bits of the physical address are set to 00.	1	0
PHY_AD1		0	0
PHY_AD0		0	0
MODE 3	Mode select bit 3	0	0
MODE 2	Mode select bit 2	0	0
MODE 1	Mode select bit 1	0	0
MODE 0	Mode select bit 0	0	1
EXT_INT_SEL	An external 10K pull-down resistor is required.	1	0
0=Pull-down, 1=Pull-up.			





Notes:

1. Differential pair P/N skew must be less than 20 mils, and the maximum trace length must be less than10 inches.
2. Using the 100Ω±10% differential impedance with 50Ω±10% single-ended impedance for SerDes traces is recommended.
3. To minimize crosstalk, the distance between separate adjacent pairs that are on the same layer must be equal to or larger than 40 mils.
4. Copper filling around transformers is prohibited for better ESD protection performance.
5. For better EMI suppression performance, do not route in top layer.

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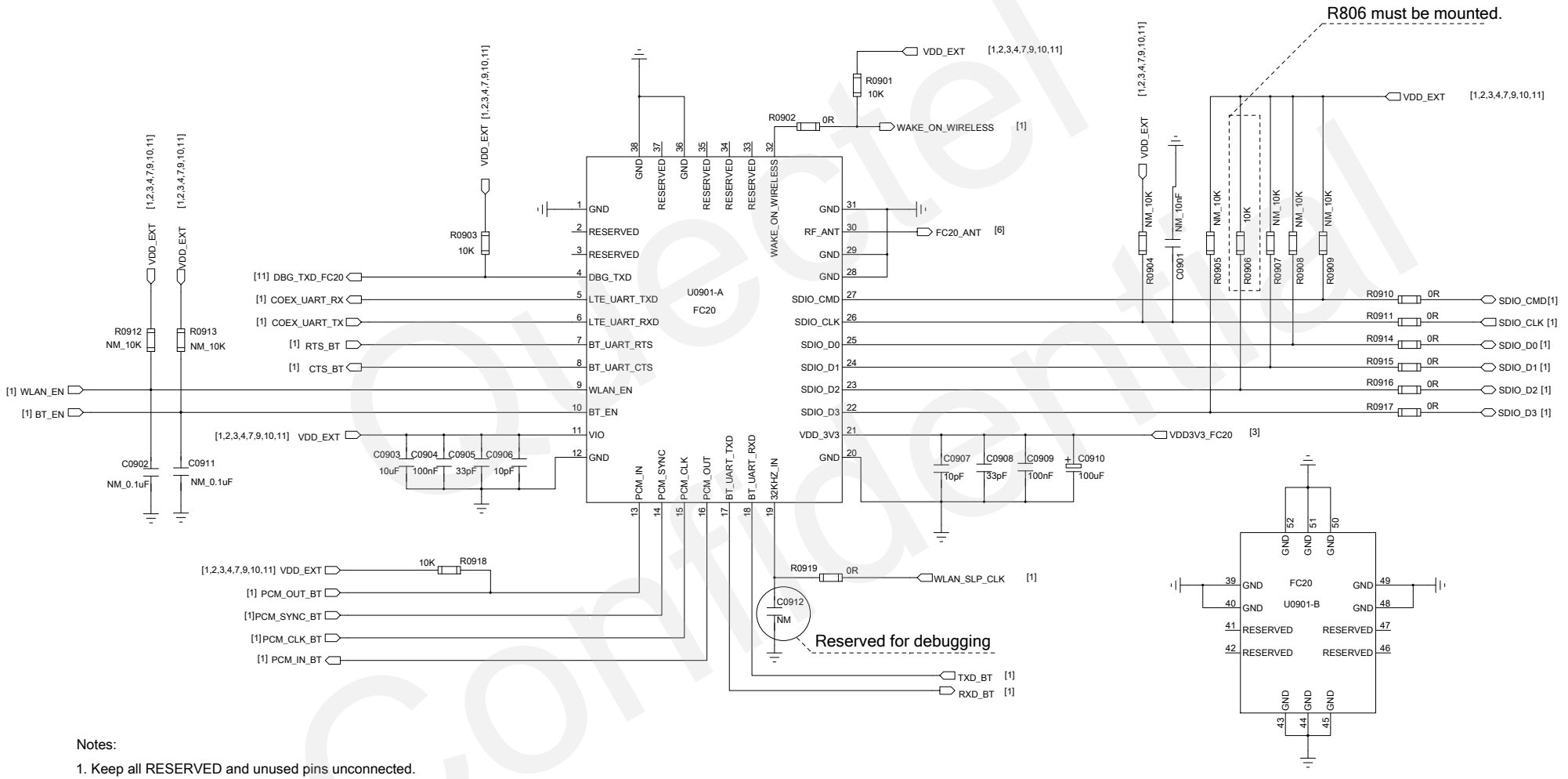
FC20 Design



Notes:

1. Keep all RESERVED and unused pins unconnected.
2. BT function of FC20 is under development.
3. SDIO_DATA2 is a signal that affects the boot of the module, and should be kept at high level when the power supply resets.
4. The impedance of the SDIO data signal line must be controlled as 50Ω when routing.
5. SDIO data lines should be wrapped together by GND lines; SDIO_CMD and SDIO_CLK network lines should be wrapped with GND lines separately.

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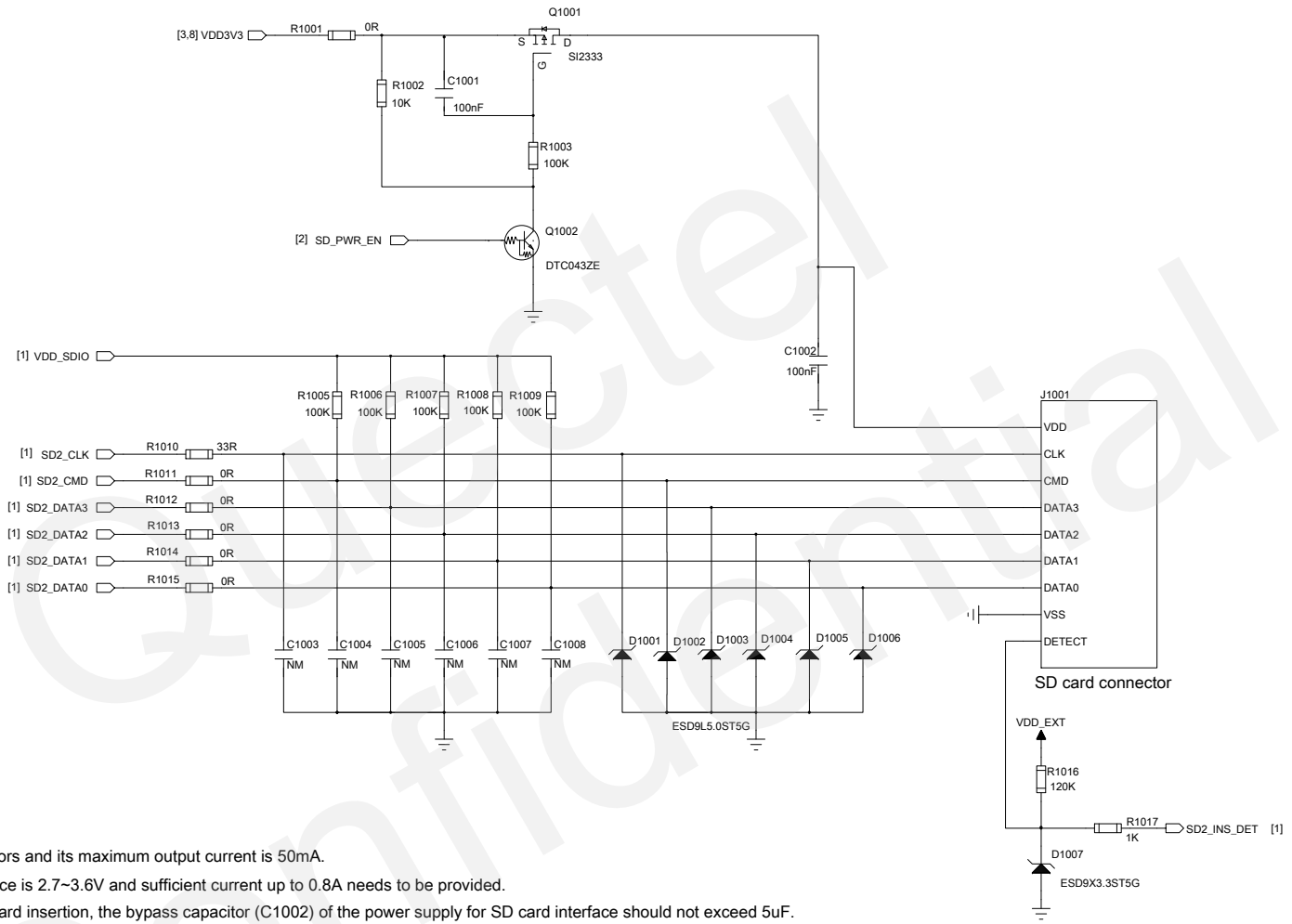
SD Card Interface Design



Notes:

1. VDD_SDIO can only be used for SDIO pull-up resistors and its maximum output current is 50mA.
2. The supply voltage range of VDD for SD card interface is 2.7~3.6V and sufficient current up to 0.8A needs to be provided.
3. To maximally limit the surge current caused by SD card insertion, the bypass capacitor (C1002) of the power supply for SD card interface should not exceed 5uF.
4. To avoid the jitter of bus, resistors R1005~R1009 are needed to pull up SDIO to VDD_SDIO. The value of these resistors is among 10~100kohm and the recommended value is 100kohm.
5. In order to improve signal quality, it is recommended to add 0Ω resistors R1010~R1015 in series between the module and the SD card connector.
   The bypass capacitors C1003~C1008 are reserved with no mounting by default. All resistors and bypass capacitors should be placed close to the module.
6. It is recommended to add ESD components near the pins of SD card connector. The parasitic capacitance of ESD components should be smaller than 15pF.
7. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock signals, DCDC signals, etc.
8. Route SD card lines with 50Ω impedance. It is important to route the SDIO signal traces with total grounding.
9. Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 40pF.
10. It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the exterior total trace length should be less than 23mm.
11. The pin DETECT of SD card connector must be connected to the module when SD card function is used.

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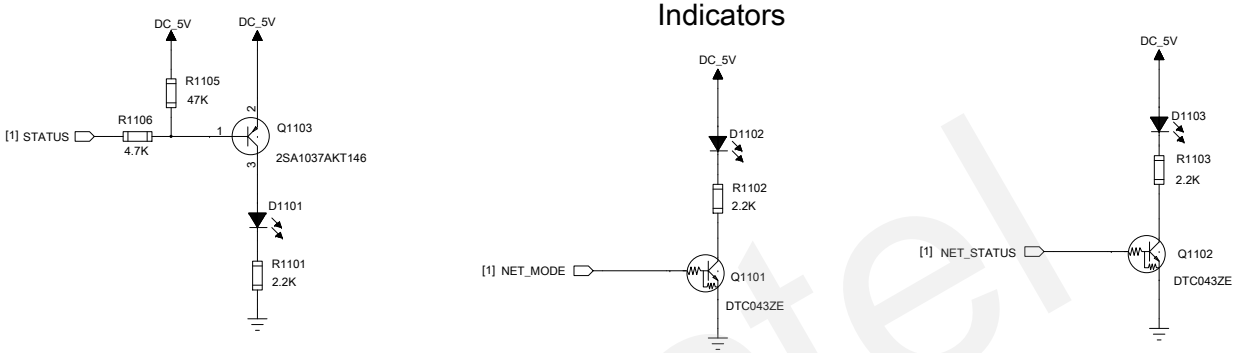
Indicators and Test Points

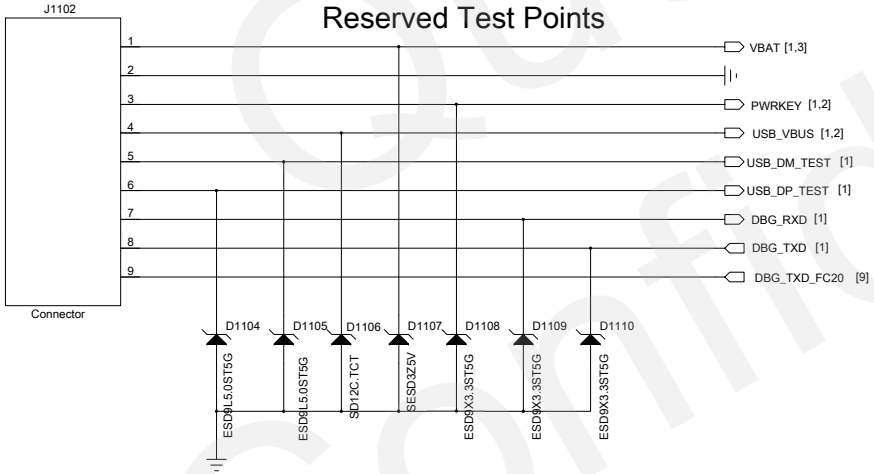
Indicators



Notes:

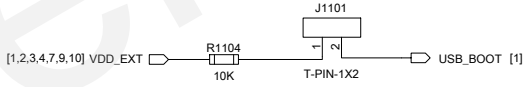
1. The STATUS is an open drain output pin, and its drive current is less than 1mA.
2. For more details about NET_MODE and NET_STATUS, please refer to *Quectel_EC25_Hardware_Design.*
3. If the current consumption is required as low as possible when the device is in sleep, replace the power supply of indicators with controllable one.
   Turn off the power when the module enters sleep mode.

Reserved Test Points



Notes:

1. Both USB and debug UART interfaces are reserved for software debugging.
2. USB interface also can be used to upgrade firmware.
3. Keep USB test points as close as possible to USB pins.
   Junction capacitance of ESD component on USB data lines might influence the signal, please pay attention to it. Typically, the capacitance should be less than 1pF.
4. DBG interfaces support 1.8V power domain.
   A level translator should be used if the power domain of customers' application is 3.3V.



Note:

USB_BOOT is kept open by default and the module will be forced into download mode when USB_BOOT is at high level.

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